MISEL – a multiband event-based intelligent vision system

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Outline

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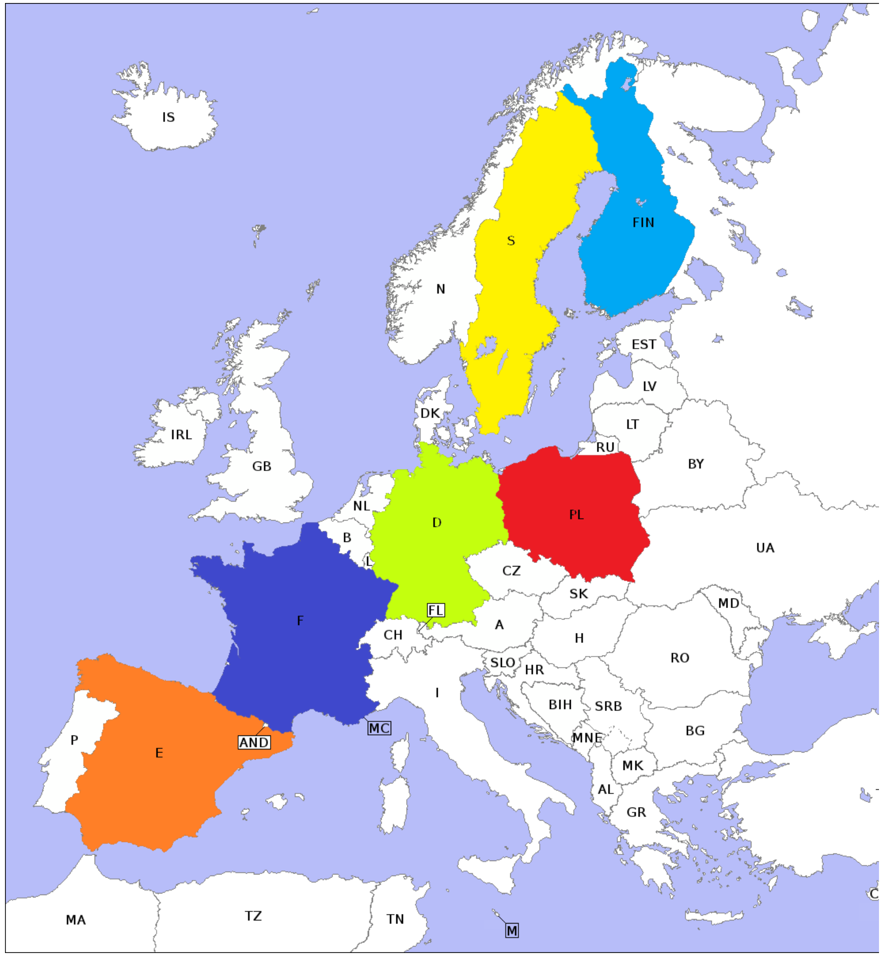
- Objectives
- System approach overview
- Cellular/cerebellar processor chip
- Cortical processor chip
- Beyond CMOS technology integration
  - – CQD-based NIR photodetector
  - – Ferroelectric memory

Project basic fact



Consortium of 9 partners from 6 European countries:

- VTT, Kovilta (Finland)
- ULUND (Sweden)
- TUL (Poland)
- AMO, BUW, Fraunhofer (Germany)
- LNE (France)
- USC (Spain)

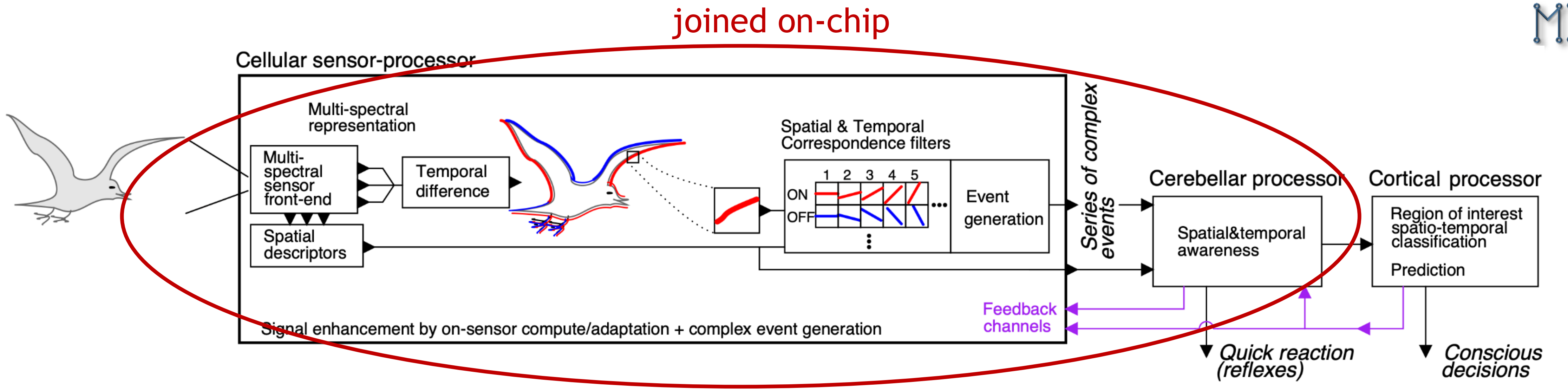
https://www.misel-project.eu/

Project objectives

Develop **standalone multiband vision system** for advanced situation awareness, which would demonstrate the advantages of the MISEL holistic sensing and computing approach over the conventional approaches.

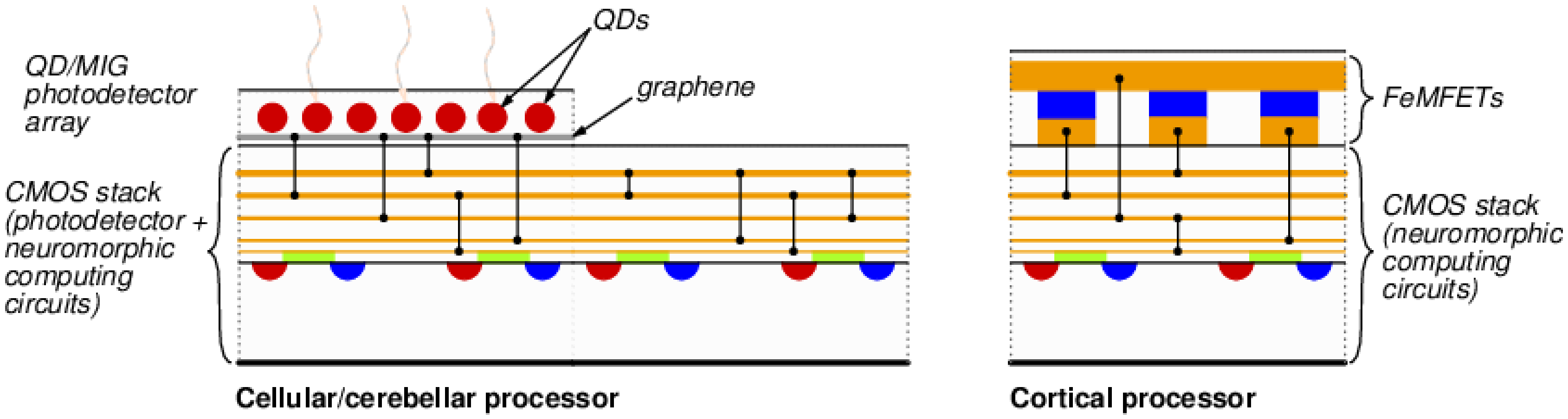
1. **Demonstrate adaptive multiband (VIS-to-NIR) pixels for the camera.**
2. **Demonstrate in-sensor computing for data reduction and adaptation.**
3. **Demonstrate FeRAM monolithically integrated on top of silicon computing layer.**
4. **Explore and implement the MISEL holistic sensing-computing approach.**
5. **Demonstrate the competitiveness of neuromorphic computing.**

System approach overview



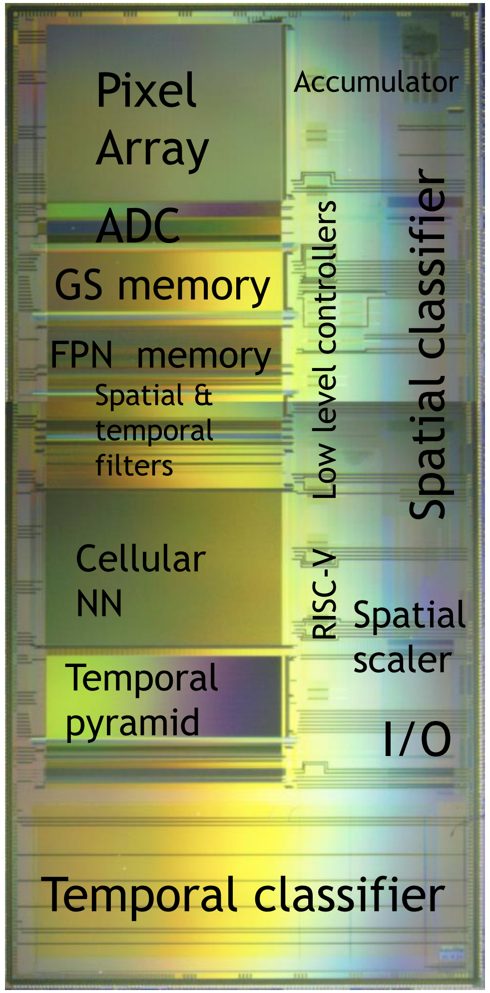
3D-integrated intelligent artificial vision system with on-chip sensing, memory and computation capacity.

Event-based computation takes place at 3 processing levels: cellular (retina), cerebellar, and cortical.



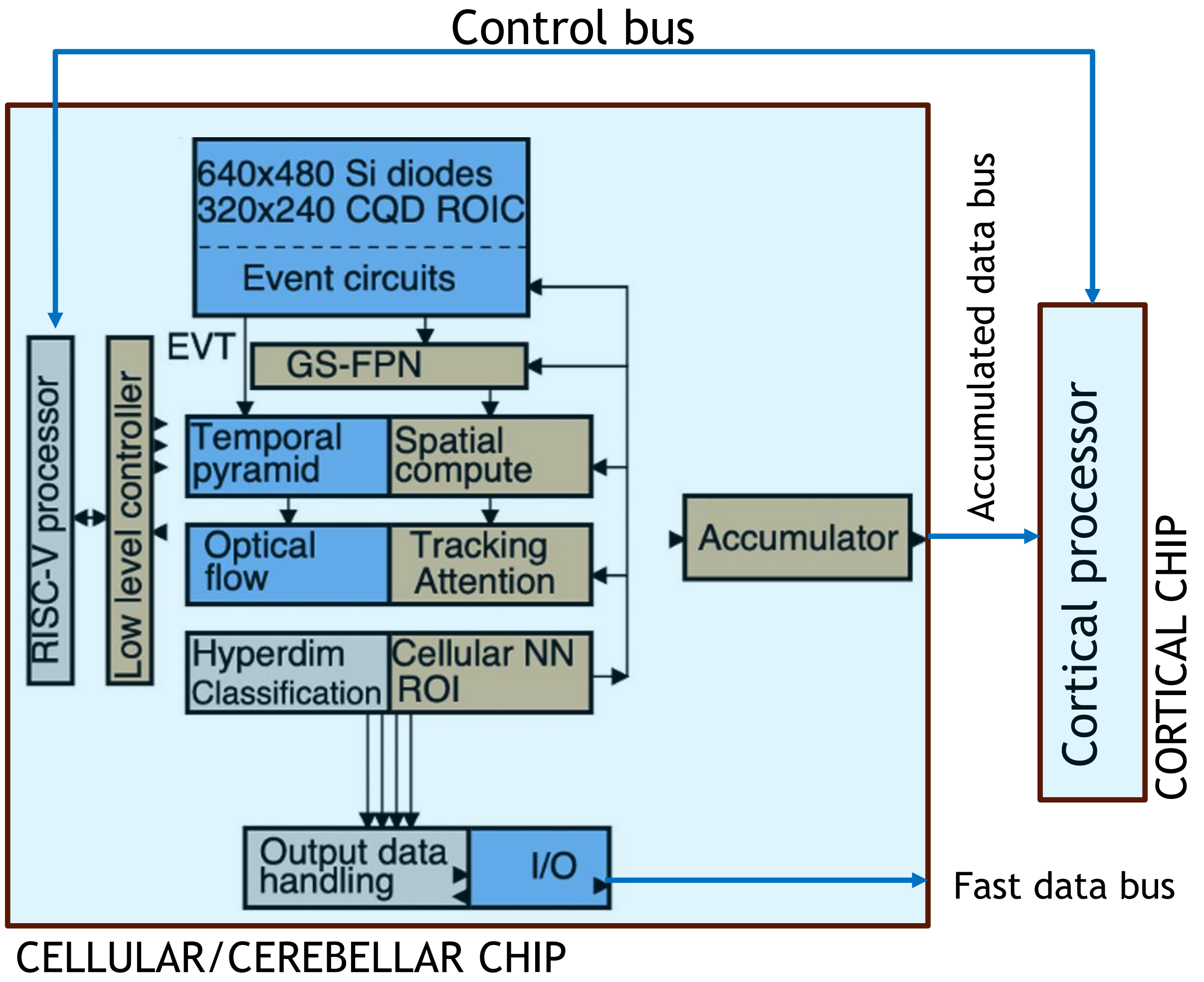
Cellular/cerebellar processor chip

- Sensing and computing on the same chip
  - Pixel array produces data at a high frame rate >1kfps
  - On-chip compute has access to the high fps data without bottlenecks associated with off-chip data transfer
- The front-end on-chip compute and memories are pitch matched to the pixel column
  - Further compute is carried out with computing accelerators at chip periphery
- Implemented in 180nm CMOS.
  - The chip dimensions are 27x13mm2.
  - The system-on-chip mixed-mode design has ~100 million transistors



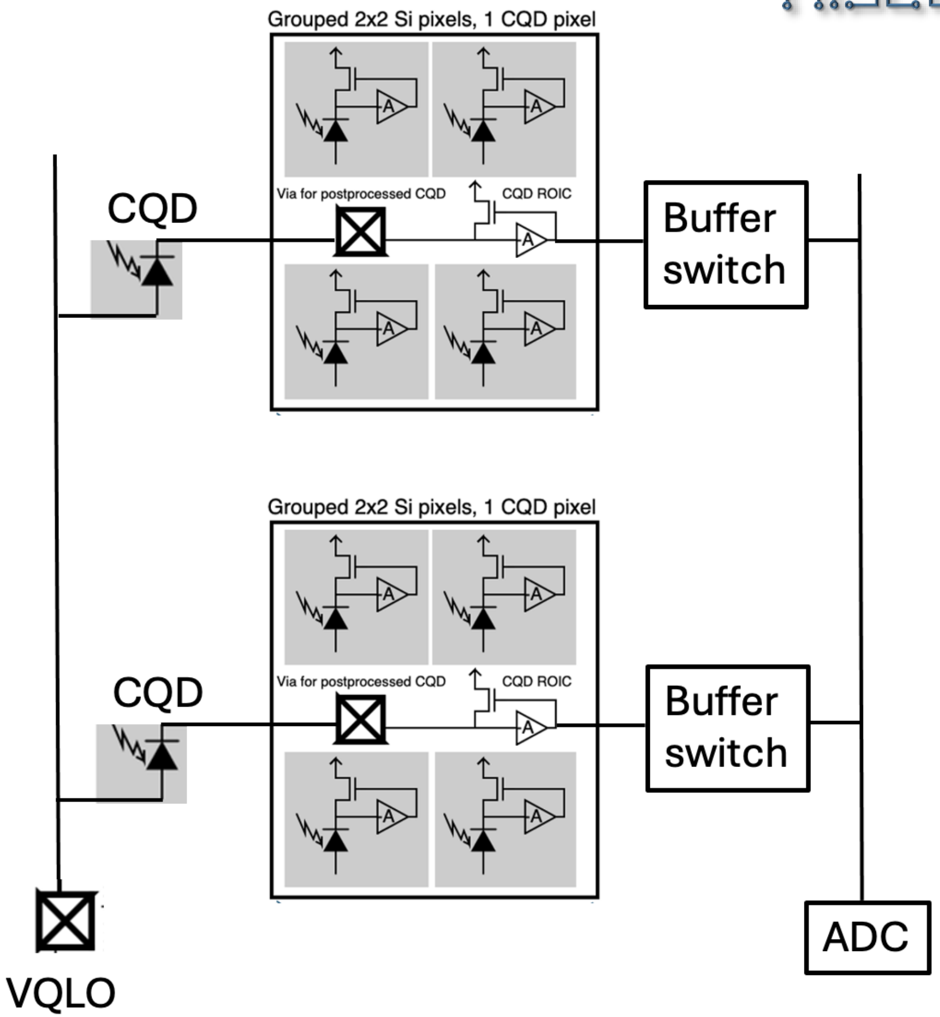
Cellular/cerebellar processor chip

- Cellular/cerebellar processor simultaneously provides
  - processing results for fast reaction
  - accumulated data for further ROI analysis with the cortical processor chip
- Accumulated data bus transfers lowered frame rate data based on requests from cortical chip
  - Accumulator collects and combines 32x32 ROI data from multiple frames and provides the data to the cortical processor.
- Fast data bus is a 64-bit general purpose bus with access to all data processing units on chip



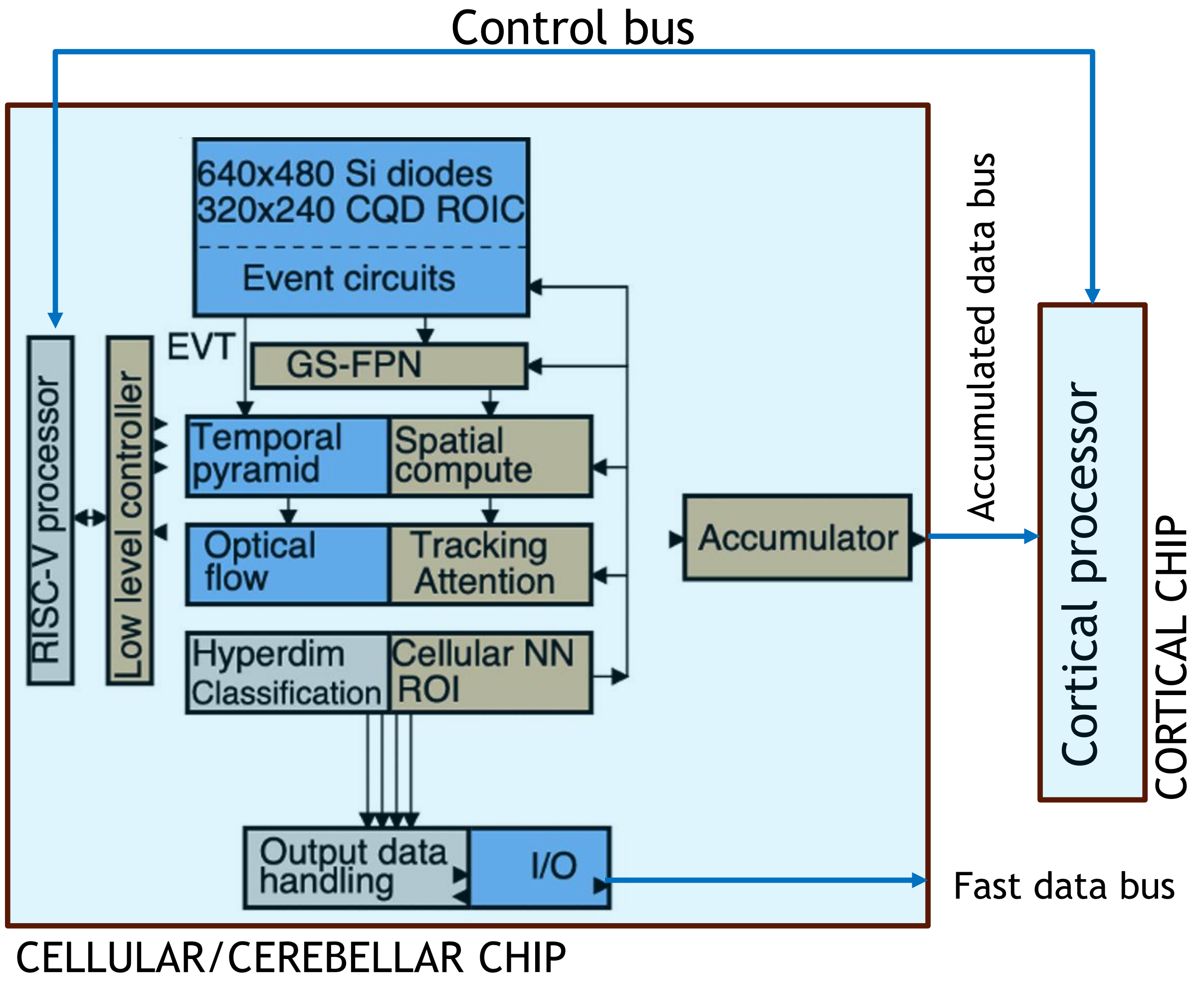
Cellular/cerebellar processor chip

- The pixels are drawn in a group of 2x2 Si pixels accompanied with an additional readout circuit for postprocessed QD-Graphene photodetectors
  - Every 2x2 pixel group has a via to postprocessing steps carried out after the CMOS
  - The dimensions of the 2x2 pixel group are 20x20um2
- Postprocessed CQDs are connected between the via in the 2x2 pixel group and a column-level via
- There are a total of 640x480 Si pixels and 320x240 colloidal quantum dot (CQD) detector readout circuits (ROIC) on the chip.
- The pixels have an active logarithmic (not integrating) sensor front end so that the pixel value is available for reading at any time
  - The negative feedback provided by the amplifier of the pixel front-end regulates the voltage at the cathode of the photodiode so that it remains at a nearly constant voltage.
- The output of the feedback amplifier is read out of the pixel array



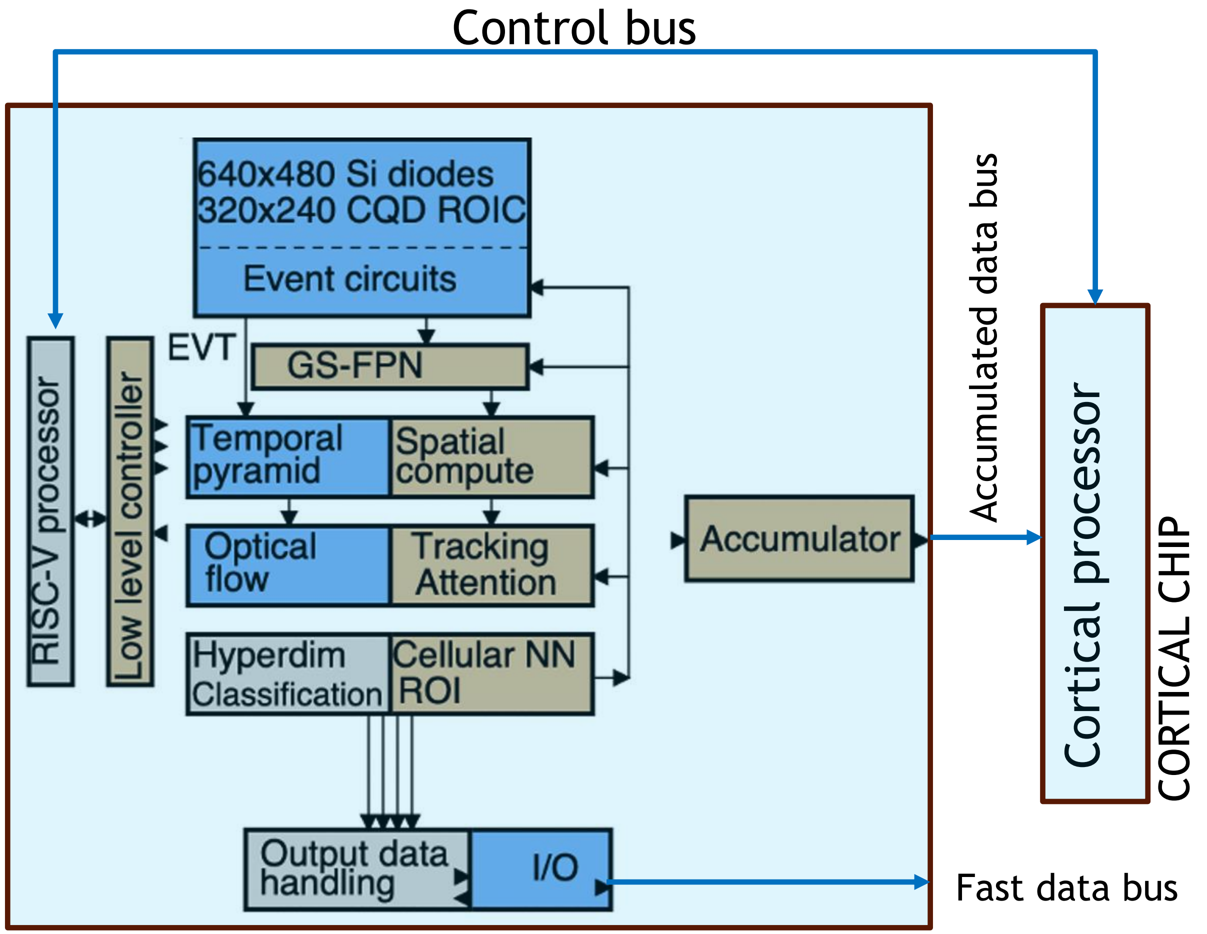
Cellular/cerebellar processor chip

- The outputs from the pixels are converted to events and intensity image with per-column event generation circuits.
  - row-wise reading out pixel-values and using ADCs to convert the difference of previous pixel values
- On-chip FPN compensation of the logarithmic sensors is with values computed from image statistics
- Supports a broad range of temporal and spatial scales to enable analysis over a wide range of object sizes and speeds of motion
  - circuitry for spatial and temporal image processing for feature and object segmentation, classification and tracking
  - A temporal event pyramid optical flow generates and stores event planes at different timescales and computes motion from those



Cellular/cerebellar processor chip

- Spatial computing is carried out to extract for example FAST corners that can be used for tracking
- There are two hyperdimensional associative processors on chip.
  - One is for object classification (64x3600 CAM cells)
  - One is for motion pattern classification (192x3600 CAM cells)
- There is a 320x240 sized image-parallel cellular neural network
  - programmable neighborhood connectivity kernels for ROI extraction and tracking
  - 21 local memories per cell for storing intermediate results
- Output data handling is capable of providing ROI data from certain part of the image and scale the data.



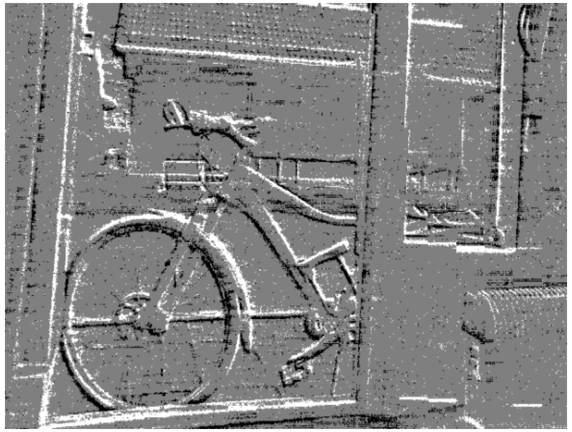
CELLULAR/CEREBELLAR CHIP

Cellular/cerebellar processor chip

- The chip has nine low level custom controllers (LLC) that are dedicated to control different parts of the chip.
  - LLCs operate at 100MHz and have 2k x 16b program memory
- RISC-V runs at 100MHz
  - Capable of initiating and halting the operation of the LLCs
  - Has access to processed data
- 640x480 images were captured with Si diodes (sensing, ADC, readout) at > 1kfps
  - intensity image data and temporal difference event data were captured
  - on-chip FPN compensation was applied
- We are now bringing up the temporal pyramid/optical flow, spatial compute, tracking, classification, ROI and accumulation operations.

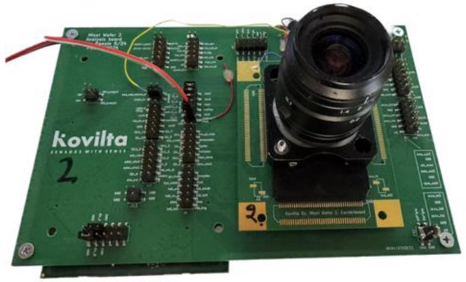
Log intensity image

Temporal difference events



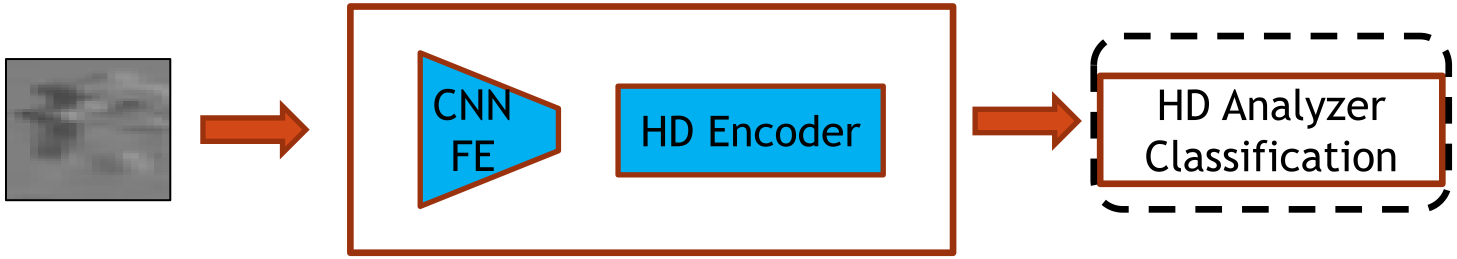
Chip carrier board

Measurement board

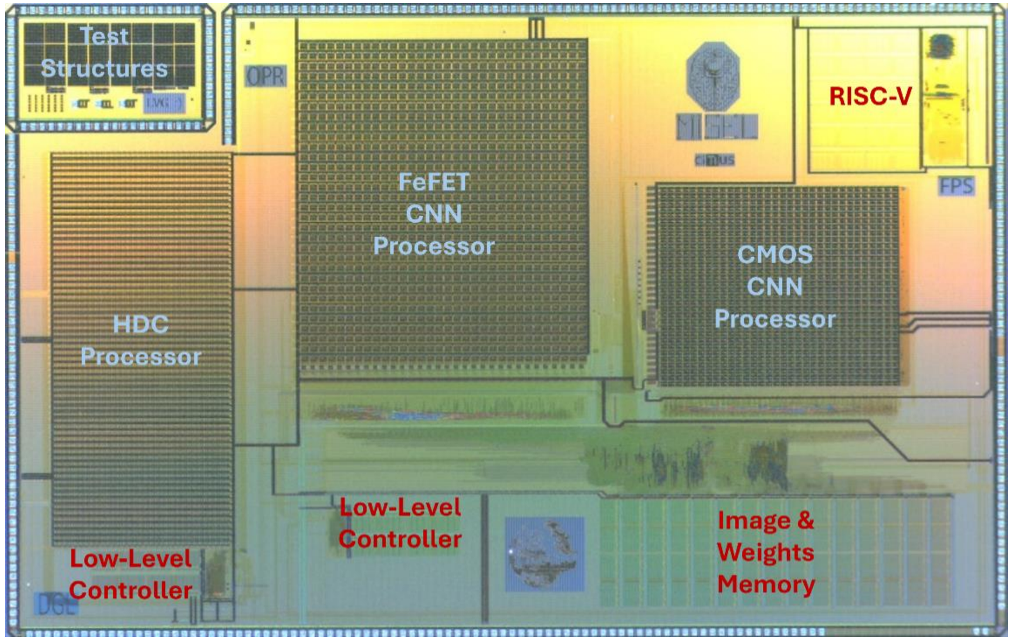


Cortical processor chip

- Cortical processor - block diagram

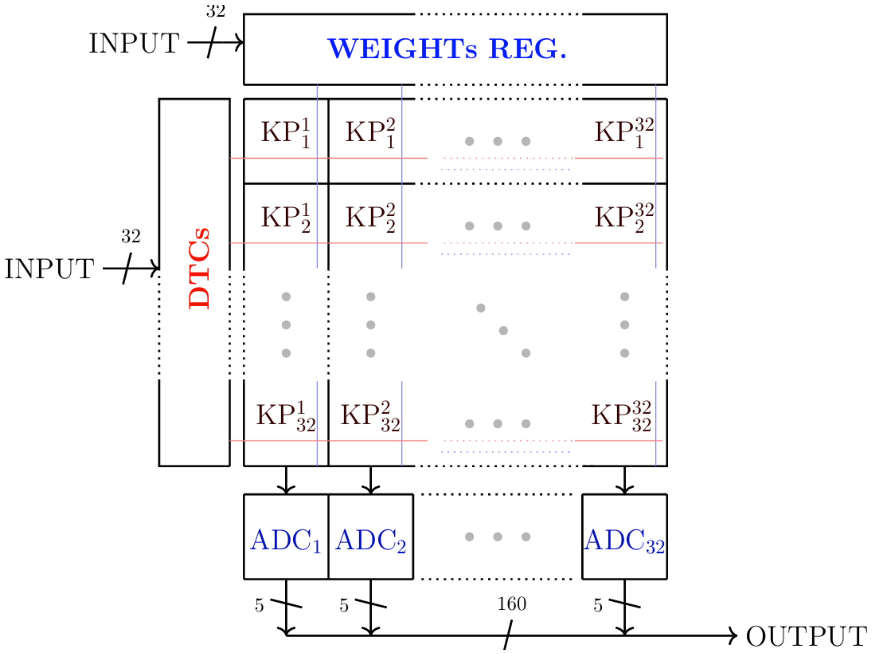


- Cortical processor - chip micrograph
  - 180nm CMOS, 7x11mm2
  - Data path
    - CNN with CMOS or CNN with CMOS + FeFET with 23x23 KPs each with 3x3 multipliers
    - HDC 2048 vectors, 32 input and 32 output channels
  - Control
    - NEORV32 RISC-V



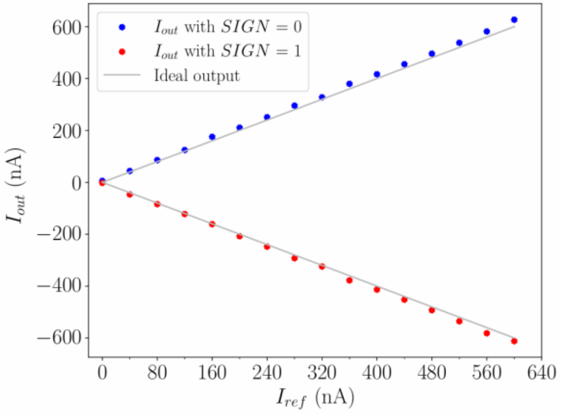
Cortical processor chip

- Experimental results – on-going

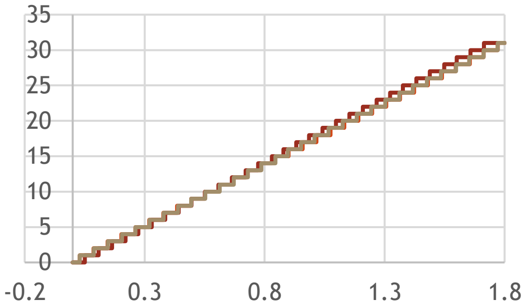


O. Pereira-Rial, H. Dahlberg et al., "*Multi-Level Analog Computing-In-Memory FeFET-based Unit Cell for Deep Learning*", **ISCAS 2025**.

Multiplier response to PWM



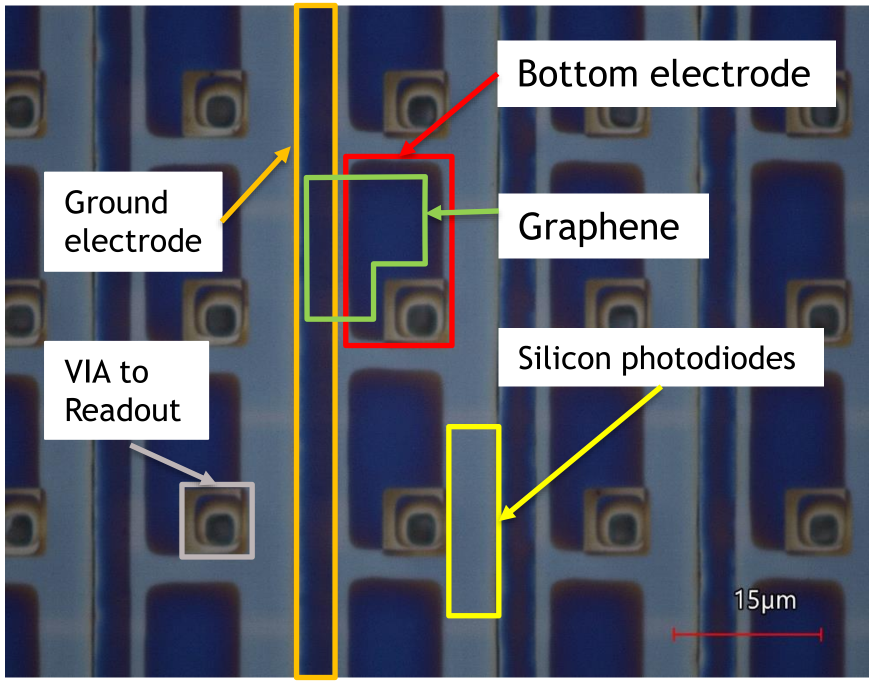
Pos. + neg. weights in CMOS + FeFET

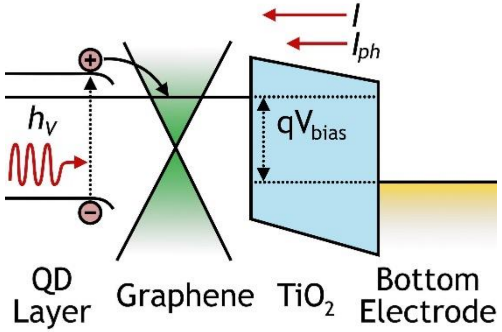


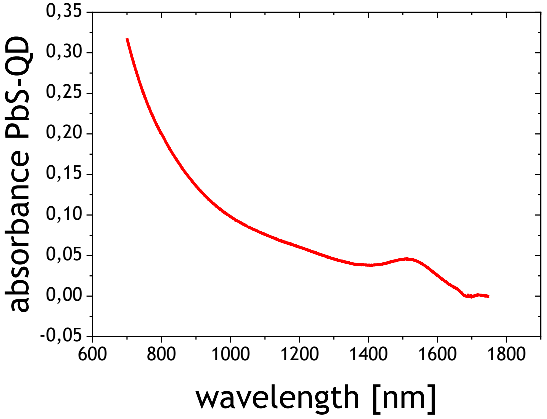
5-bit SAR ADC output for full 1.8V range @5MHz

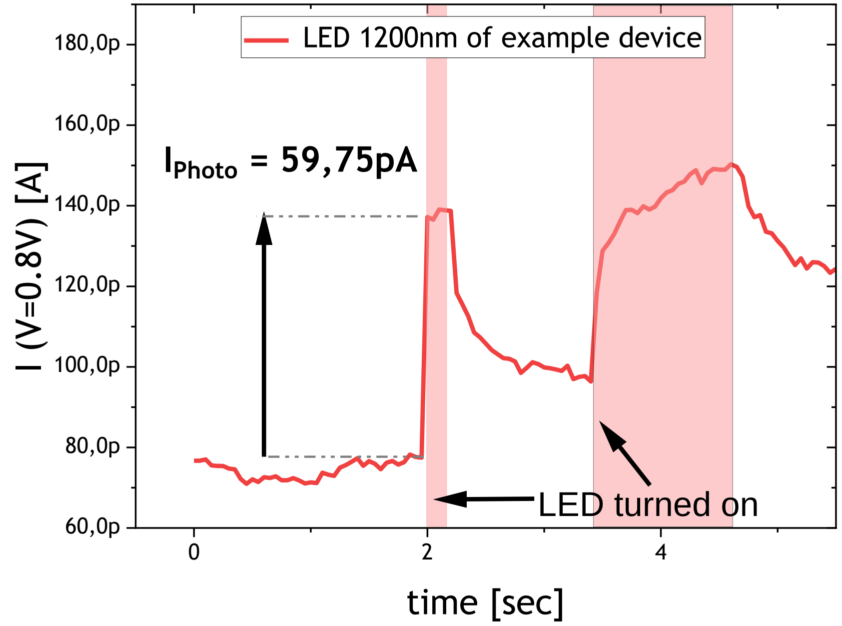
NLE <0.2LSB

Beyond CMOS – QD-Graphene photodetector









- Biased **M**etal **I**nsulator **G**raphene **(MIG)** Diodes create a tunnel current through TiO2
- QD absorption layer adds electrons to the Graphene when illuminated resulting in a Photocurrent
- QDs can be specialized to absorb infrared light
- Advantages: ability to be integrated on top of CMOS chip as well low dark currents

Beyond CMOS - ferroelectric memory

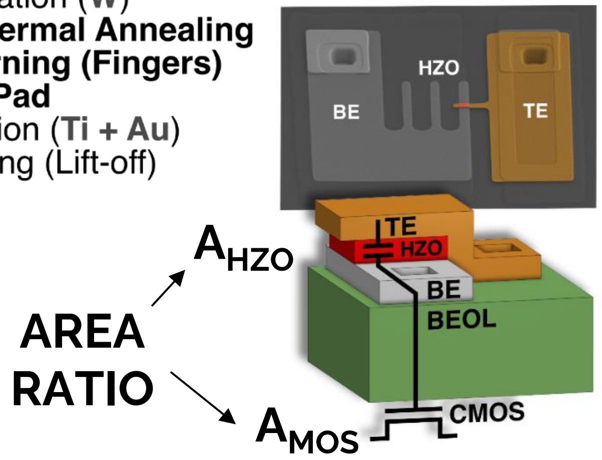
LUND UNIVERSITY

VTT

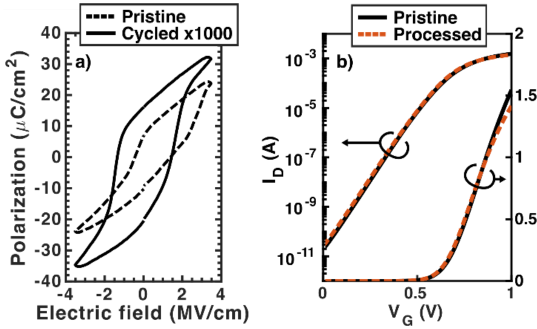
MISEL

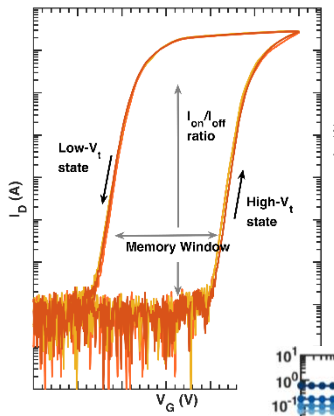
Processing

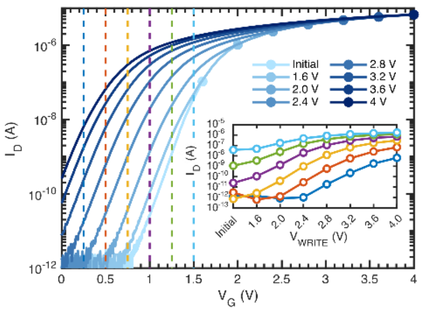
- **XFAB Processing**
- **Top Spacer Via**
  - Definition
  - Etch
  - Metallization (**TiW**)
- **Bottom Electrode**
  - Depostion (**TiN**)
  - Patterning (Fingers)
- **HZO Deposition**
- **Top Eectrode**
  - Deposition (**W**)
  - Patterning (HZO etch mask)
- **HZO Removal**
  - Etching
  - Metallization (**W**)
- **Rapid Thermal Annealing**
- **TE Patterning (Fingers)**
- **Probing Pad**
  - Deposition (**Ti + Au**)
  - Patterning (Lift-off)

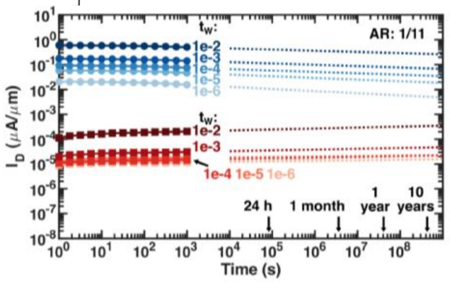


Post-processing & FeFET behaviour





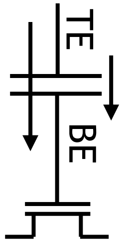




Impact of Area Ratio (AR)

TE to BE Charge Injection (CI)

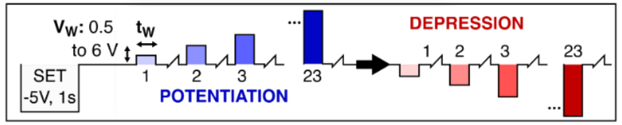
- Pulse length dependent
- Field dependent

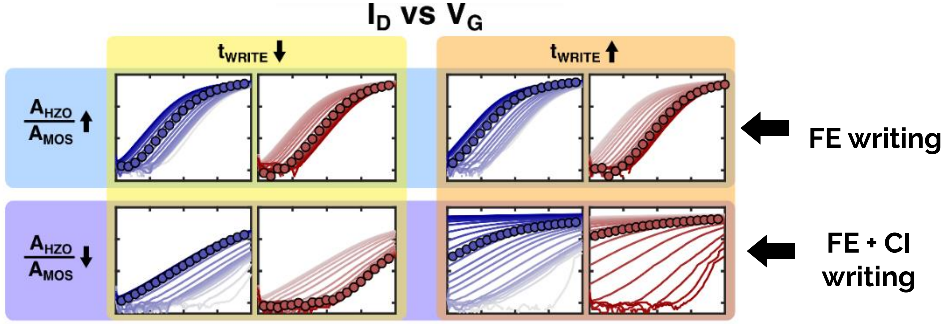


Ferroelectric (FE) Polarization

- Field dependent

$$V_{FE} = \frac{V_G}{1 + C_{FE}/C_{MOS}}$$





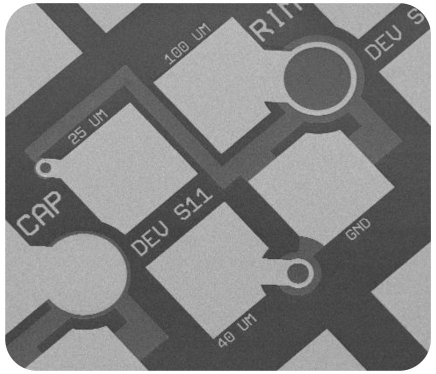
- CMOS BEOL-compatible processing of FeFET devices
- Analog writing & state retention
- AR is a highly flexible parameter impacting dynamics

H. Dahlberg *et al.*, *IEEE Access* (2025) - DOI: 10.1109/ACCESS.2025.3527628
Ó.Pereira-Rial *et al.*, ISCAS (2025) - DOI: xxxxx

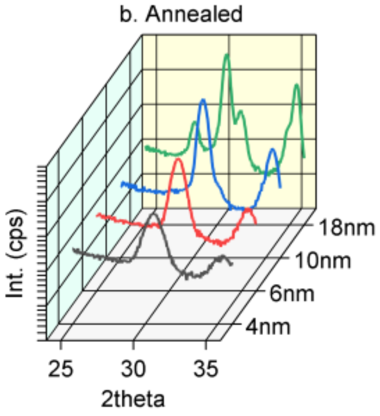
Beyond CMOS - ferroelectric memory

- VTT has optimized ~5 nm thick HZO FE-stacks
  - Annealing with and without top electrode
  - Targeting thin-film FeFET integration; semiconductive oxide, carbon nanotube or 2D material
- Very good switching stability
  - Uniform distribution
  - Distinct analogue states
  - Low switching fatigue
- BEOL with VTT designed ASIC
  - Ultra-energy-efficient CIM for AI

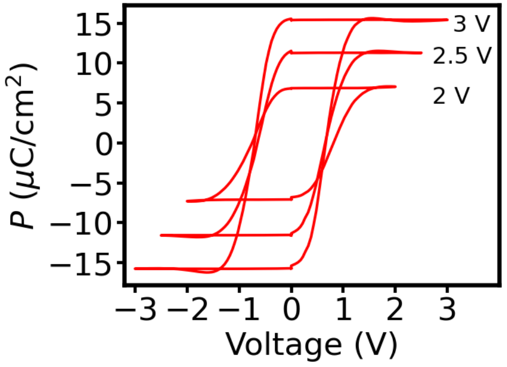
Fabricated FE-caps



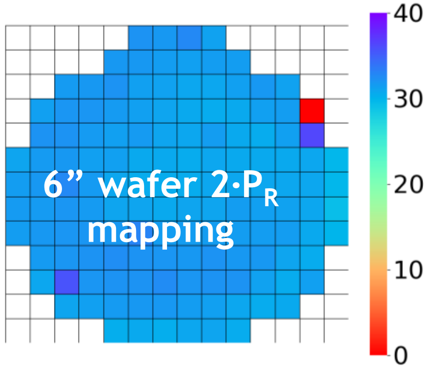
Optimized stack and annealing



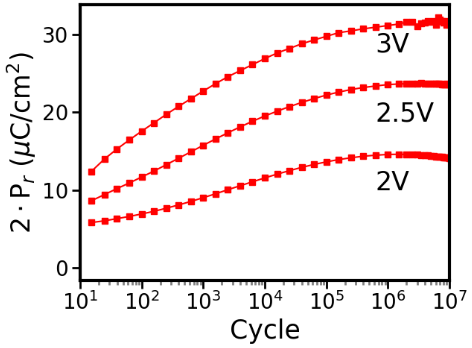
Characterized Polarization



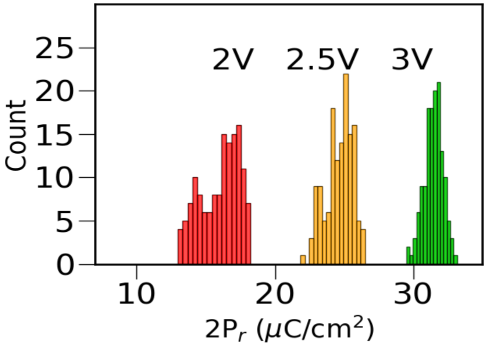
High wafer uniformity post wakeup



Low fatigue switching endurance



Tight wafer distribution of analogue states



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